EXHIBIT A

KWUN BHANSALI LAZARUS

Nikki Hueston <nhueston@kblfirm.com>

Disclosure of Dr. Jose Renau under the Protective Order

Seeve, Brian <bseeve@princelobel.com> Fri, May 27, 2022 at 1:50 PM
To: Asim Bhansali <abhansali@kblfirm.com>, "Nathan R. Speed" <nathan.speed@wolfgreenfield.com>, Matthias Kamber <mkamber@keker.com>, Michelle Ybarra <mybarra@keker.com>
Cc: Singular <Singular@princelobel.com>

Counsel –

Pursuant to ¶11(a) of the Protective Order, we seek to disclose Jose Renau for the review of Protected Material. Attached please find Dr. Renau's current CV and a list of current and past employment and consulting relationships. Dr. Renau has not testified at trial or in deposition within the last five years.

Best,

- Brian

2 attachments

renauCV.pdf
167K

Renau_Employment.pdf
49K

Personal Information

Jose Renau
Santa Cruz, CA 95064

Email renau@ucsc.edu
Phone (831) 295-3641

`Jul 2016-present` Professor. University of California, Santa Cruz.
`Jul 2010-2016` Associate Professor. University of California, Santa Cruz.
`Jul 2004-2010` Assistant Professor. University of California, Santa Cruz.
`Jan 1999-Jun 2003` Research Assistant. University of Illinois at Urbana-Champaign.
`Aug 1998-Dec 1998` System Administrator. University of Illinois at Urbana-Champaign.
`Jan 1998-Jul 1998` Computer Network Specialist. FIHOCA, S.A. (Spain).
`Sep 1996-Sep 1997` System Administrator. Asertel, S.A. (Spain).
`May 1995-Sep 1996` Systems Manager. Ramon Lull University (Spain).

Education

University of Illinois at Urbana Champaign: (Advisor: Professor Josep Torrellas)

2004 Ph.D. Computer Science, University of Illinois at Urbana Champaign.
Thesis: *"Chip Multiprocessor with Thread Level Speculation: Performance and Energy"*

1999 M.S. Computer Science, University of Illinois at Urbana Champaign.
Thesis: *"Memory Hierarchies in Intelligent Memories: Energy/Performance Design"*

Ramon Llull University, Spain:

1997 M.S. Computer Engineering, Ramon Llull University (Spain)
Thesis: *"Linux Kernel IEEE1284 (parallel port) Implementation"*

1994 B.S. Computer Science, Ramon Llull University (Spain)
Final project: *"ILZR, a New Data Compression Algorithm"*

Awards and Funding

- 2021, AMD cash gift ($50K)
- 2020, Google faculty award ($50K)
- 2019, PI A Productive Open Source Hardware Development Flow ($1.2M)
- 2015, co-PI NIH Non-Invasive Magnetic Nanothermotherapy for the Resolution of Wound Biofilm Infection ($50K)
- 2015, co-PI NSF Efficient Cascode Power Supply Systems ($285K)
- 2013, PI NSF XPS Cooperative Deterministic Concurrency ($750K)
- 2013, PI NSF CSR Rethinking the Memory Hierarchy ($500K)
- 2013, Intel Gift ($10K)
- 2012, PI NSF CRI:Fast Performance, Power and Thermal Modeling for Heterogeneous System ($300K)
- 2011, PI NSF CRI: Prototyping Platform to Enable Power-Centric Multicore Research ($120K)

- 2010, AMD gift ($10K)
- 2010, PI NASA/UARC, *Dynamically Adaptable Computers for Renewable Energy Powered Data Centers* ($25k)
- 2009, SUN cash gift ($75K)
- 2008, NVIDIA cash gift ($70K)
- 2008, PI NSF CRI: IAD Temperature Measurement Infrastructure for Power, Variability, and Reliability Analysis ($275K)
- 2007, PI NSF SMA: Accurate Temperature Measurement Infrastructure and Methodology for Power, Variability, and Reliability Analysis. (co-PI are Ali Shakouri, Matthew Gutthaus, Steve Kang, and Michael Huang) ($300k UCSC + $100k Rochester)
- 2007, PI NASA/UARC, *Radiation Tolerant FPGA Processor* ($25k)
- 2007, SUN Academic Excellence Award ($110K)
- 2007, co-PI Special Research Grant from UCSC (PI is Matthew Gutthaus) ($20k)
- 2007, Xilinx University Donation Software ($8k)
- 2006, co-PI IES Berkeley/France Fund Award (co-PI is Albert Cohen) ($9k)
- 2006, PI Special Research Grant from UCSC ($12k)
- 2006, PI NASA/UARC ($50k) *Checkpointed Fault Tolerant FPGA Systems*
- 2006, PI NSF CAREER ($400k) *Understanding, Estimating, and Reducing Processor Design Complexity*
- 2006, SUN equipment (Niagara server $16k)
- 2006, Altera equipment (Stratix II DSP board $5k)
- 2006, IEEE Micro Top Picks in Computer Architecture
- 2005, PI DARPA PERCS subcontract ($20k)
- 2003, IBM Graduate Research Fellowship
- 2003, J. Poppelbaum Memorial Award, University of Illinois

Students

- Current Phd: Ramesh Jayaraman (15-), Nursultan Kabylkas (16-), Sheng Hong Wang (17-), Sakshi Garg (20-), Bhawandeep Singh (20-), Jing-Hsiang Huang (21-),
- Current MS: Micaela Kapp (19-), Sloan Liu (20-), Abdullah Al-Omari (21-)

Alumni:

- PhD: Javi Martinez (04-07), Cyrus Bazeghi (04-08), Sangeetha Nair (05-11), Sean Halle (04-11), David Munday (07-13), Ehsan Ardestani (08-14), Madan Das (08-15), Alamelu Sankaranarayanan (06-16), Gabriel Southern (08-16), Elnaz Ebrahimi (09-17), Haven Skinner (11-18), Rafael Trapani Possignolo (12-18), Daphne Gorman (12-18) Akash Sridhar (14-21)
- MS: Shantanu Kale (05-06), Liying Su (05-06), David Brian Van Der Bokke (05-06), Suraj Narender (05-07), Angela Schmid (06-07), Matt Fischler (06-07), Melisa Nuñez (05-08), Joseph Nayfach (05-08), Keertika Singh (08-09), Michael Brown (06-11), Raj Maitra (12-12), Pranav Natesh (10-12), Ian Lee (09-12), Jason Duong (09-13), Vidyuth Srivatsaa (10-13), Christopher Hoseit

(12-13), Himabindu Thota (12-13), Gregory Jackson (09-15), Ethan Papp (14-15), Sina Hassani (13-15), Azzam Ahamd Qureshi* (15-16), Xue Jingwen (16-16), Xuan Gu* (16-16), Zhiguang Cheng (16-16), Junheng Chen (16-16), Rigo Dicochea (07-16), Arun Suresh* (15-16), Vishnu Surya Reddy Nandi (17), Yuxiong Zhu (17), Garvit Rajendra Mantri (16-18), Yuxun Qiu (17-18), Rohan Ganpati (17-19), Qian Chen (19-19), Rohan Jobanputra (18-19), Huijie Pan (18-20), Joshua Pena (19-20), Kenneth Mayer (19-20), Hunter Coffman (19-20), Arik Yueh (20-21), Oly Kebede (21)

Publications

Conferences

[1] Effective Processor Verification with Logic Fuzzer Enhanced Co-simulation, Nursultan Kabylkas, Tommy Thorn (Esperanto Technologies), Shreesha Srinath (Intel), Polychronis Xekalakis (Nvidia), and Jose Renau. 54th International Symposium on Microarchitecture (MICRO), October 2021.

[2] LiveSim: A Fast Hot Reload Simulator, Haven Skinner, Rafael T. Possignolo, Sheng-Hong Wang, and Jose Renau, International Symposium on Performance Analysis of Systems and Software (ISPASS), April 2020.

[3] EMI Architectural Model and Core Hopping, Daphne I. Gorman, Rafael T. Possignolo, and Jose Renau. 52th International Symposium on Microarchitecture (MICRO), October 2019.

[4] SMatch: Structural Matching for Fast Resynthesis in FPGAs, Rafael T. Possignolo, and Jose Renau, Design Automation Conference (DAC), June 2019.

[5] *Liam: An Actor Based Programming Model for HDLs*, Haven Skinner, Rafael T. Possignolo, and Jose Renau. 15th ACM-IEEE International Conference on Formal Methods and Models for System Design (**MEMOCODE**), October 2017.

[6] *Architectural Opportunities for Novel Dynamic EMI Shifting (DEMIS)*, Daphne I. Gorman, Jose Renau, and Matthew Guthaus. 50th International Symposium on Microarchitecture (**MICRO**), October 2017.

[7] *LiveSynth: Towards an Interactive Synthesis Flow*, Rafael Trapani Possignolo, and Jose Renau, Design Automation Conference (**DAC**), June 2017.

[8] *Timing Speculative SRAM*, Elnaz Ebrahimi, Matthew Guthaus, and Jose Renau, International Symposium on Circuits and Systems (**ISCAS**), May 2017.

[9] *Level Shifter Design for Voltage Stacking*, Elnaz Ebrahimi, Rafael Trapani Possignolo, and Jose Renau, International Symposium on Circuits and Systems (**ISCAS**), May 2017.

[10] *Overhead of Deoptimization Checks in the V8 JavaScript Engine*, Gabriel Southern and Jose Renau, International Symposium on Workload Characterization (**IISWC**), July 2016.

[11] *Fluid Pipelines: Elastic Circuitry meets Out-of-Order Execution*, Rafael Trapani Possignolo, Elnaz Ebrahimi, Haven Skinner, and Jose Renau, International Conference on Computer Design (**ICCD**), June 2016.

[12] *SRAM Voltage Stacking*, Elnaz Ebrahimi, Rafael Trapani Possignolo, and Jose Renau, International Symposium on Circuits and Systems (**ISCAS**), May 2016.

[13] *Analysis of PARSEC Workload Scalability*, Gabriel Southern and Jose Renau, International Symposium on Performance Analysis of Systems and Software (**ISPASS**), April 2016.

[14] *LiveSim: Going Live with Microarchitecture Simulation*, Sina Hassani, Gabriel Southern and Jose Renau, International Symposium on High-Performance Computer Architecture (**HPCA**), February 2016.

[15] *An Energy Efficient GPGPU Memory Hierarchy with Tiny Incoherent Caches*, Alamelu Sankaranarayanan, Ehsan K.Ardestani, Jose Luis Briz, and Jose Renau, International Symposium on Low Power Electronics and Design (**ISLPED**), September 2013.

[16] *ESESC: a Simulator for Time-Based Sampling of Heterogeneous Multithreaded Systems*, Ehsan K.Ardestani and Jose Renau, International Symposium on High Performance Computer Architecture (**HPCA**) ,February 2013.

[17] *Thermal-Aware Sampling in Architectural Simulation*, Ehsan K.Ardestani, Elnaz Ebrahimi, Gabriel Southern, and Jose Renau, International Symposium on Low Power Electronics and Design (**ISLPED**), August 2012.

[18] *Enabling Power Density and Thermal-Aware Floorplanning*, Ehsan K. Ardestani, Amirkoushyar Ziabari, Ali Shakouri, and Jose Renau, 28th Annual Thermal Measurement, Modeling and Management Symposium (**SEMITHERM**), March 2012.

[19] *Releasing Efficient Beta Cores to Market Early*, Sangeetha Sudhakrishnan, Rigo Dicochea, and Jose Renau, International Symposium on Computer Architecture (**ISCA**), June 2011.

[20] *Fast Thermal Simulators for Architecture Level Integrated Circuit Design*, Amirkoushyar Ziabari, Ehsan K. Ardestani, Jose Renau, and Ali Shakouri, 27th Annual Thermal Measurement, Modeling and Management Symposium (**SEMITHERM**), March 2011.

[21] *A Design Time Simulator for Computer Architects*, Sangeetha Sudhakrishnan, Francisco J. Mesa-Martinez, and Jose Renau, IEEE International Symposium on Quality Electronic Design (**ISQED**), March 2011. (Best paper award)

[22] *Characterizing Processor Thermal Behavior*, Francisco J. Mesa-Martinez, Ehsan Ardestani, and Jose Renau, Fifteenth International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), March 2010.

[23] *Cooling Solutions for Processor Infrared Thermography*, Ehsan Ardestani, Francisco J. Mesa-Martinez, and Jose Renau, 26th Annual Thermal Measurement, Modeling and Management Symposium (**SEMITHERM**), February 2010.

[24] *Processor Verification with hwBugHunt*, Sangeetha Sudhakrishnan, Liying Su,

and Jose Renau, IEEE International Symposium on Quality Electronic Design (**ISQED**), March 2008.

[25] *Effective Optimistic-Checker Tandem Core Design Through Architectural Pruning*, Francisco J. Mesa-Martinez and Jose Renau, 40th International Symposium on Microarchitecture (**MICRO**), December 2007.

[26] *Estimating Design Time for System Circuits*, Cyrus Bazeghi Francisco J. Mesa-Martinez, Brian Greskamp, Josep Torrellas, and Jose Renau, 15th IFIP International Conference on Very Large Scale Integration (**VLSI-SoC**), October 2007.

[27] *Power Model Validation Through Thermal Measurements*, Francisco J. Mesa-Martines, Joseph Nayfach-Battilan, and Jose Renau, 34th International Symposium on Computer Architecture (**ISCA**), June 2007.

[28] *SEED: Scalable, Efficient Enforcement of Dependences*, Francisco J. Mesa-Martinez, Michael C.Huang, and Jose Renau, 15th International Conference on Parallel Architectures and Compilation Techniques (**PACT**), September 2006.

[29] *POSH: A TLS Compiler that Exploits Program Structure*, Wei Liu, James Tuck, Luis Ceze, Wonsun Ahn, Karin Strauss, Jose Renau and Josep Torrellas, ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (**PPoPP**), March 2006.

[30] *uComplexity: Estimating Processor Design Effort*, Cyrus Bazeghi, Francisco J. Mesa-Martinez, and Jose Renau. 38th International Symposium on Microarchitecture (**MICRO**), November 2005.

[31] *POSH: A Profiler-Enhanced TLS Compiler that Leverages Program Structure*, Wei Liu, James Tuck, Luis Ceze, Karin Strauss, Jose Renau, and Josep Torrellas. The Second Watson Conference on Interaction between Architecture, Circuits, and Compilers (**P=AC2**), September 2005.

[32] *Thread-Level Speculation on a CMP Can Be Energy Efficient*, Jose Renau, Karin Strauss, Luis Ceze, Wei Liu, Smruti Sarangi, James Tuck, and Josep Torrellas. International Conference on Supercomputing (**ICS**), June 2005.

[33] *Tasking with Out-of-Order Spawn in TLS Chip Multiprocessors: Microarchitecture and Compilation*, Jose Renau, James Tuck, Wei Liu, Luis Ceze, Karin Strauss, and Josep Torrellas. International Conference on Supercomputing (**ICS**), June 2005.

[34] *Programming the FlexRAM Parallel Intelligent Memory System*, Basilio Fraguela, Jose Renau, Paul Feautrier, David Padua, and Josep Torrellas, International Symposium on Principles and Practice of Parallel Programming (**PPoPP**), June 2003.

[35] *Positional Adaptation of Processors: Application to Energy Reduction*, Michael Huang, Jose Renau, and Josep Torrellas, International Symposium on Computer Architecture (**ISCA**), June 2003.

[36] *Cherry: Checkpointed Early Resource Recycling in Out-of-order Microprocessors*, José F. Martínez, Jose Renau, Michael Huang, Milos Prvulovic, and Josep Torrellas, International Symposium on Microarchitecture (**MICRO**), November 2002.

[37] *Energy-Efficient Hybrid Wakeup Logic*, Michael Huang, Jose Renau, and Josep Torrellas, International Symposium on Low Power Electronics and Design (**ISLPED**), August 2002.

[38] *Cache Decomposition for Energy-Efficient Processors*, Michael Huang, Jose Renau, Seung-Moon Yoo, and Josep Torrellas, International Symposium on Low Power Electronics and Design (**ISLPED**), August 2001.

[39] *A Framework for Dynamic Energy Efficiency and Temperature Management*, Wei Huang, Jose Renau, Seung-Moon Yoo, and Josep Torrellas, International Symposium on Microarchitecture (**MICRO**), December 2000.

Journals and Patents

[40] LiveHD: A Productive Live Hardware Development Flow, Sheng-Hong Wang, Rafael T. Possignolo, Haven Blake Skinner, and Jose Renau, IEEE Micro magazine (MICRO Magazine), June 2020.

[41] GPU NTC Process Variation Compensation with Voltage Stacking, Rafael T. Possignolo, Elnaz Ebrahimi, Ehsan Ardestani, Alamelu Sankaranarayanan, Jose Luis Briz, Jose Renau. IEEE Transactions on Very Large Scale Integration Systems (TVLSI), 2018.

[42] *Managing Mismatches in Voltage Stacking with CoreUnfolding*, Ehsan K. Ardestani, Rafael Trapani Possignolo, Jose Luis Briz, and Jose Renau, ACM's Transactions on Architecture and Code Optimization (**TACO**), September 2015.

[43] *Section Based Program Analysis to Reduce Overhead of Detecting Unsynchronized Thread Communication*, Madan Das, Gabriel Southern and Jose Renau, ACM's Transactions on Architecture and Code Optimization (**TACO**), March 2015.

[44] *Sampling in Thermal Simulation of Processors: Measurement, Characterization, and Evaluation*, Ehsan K.Ardestani, Francisco J. Mesa-Martinez , Gabriel Southern , Elnaz Ebrahimi , Jose Renau IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), August 2013.

[45] *Real-time control for Keck Observatory next-generation adaptive optics*, Marc Reinig, Donald Gavel, Ehsan Ardestani, Jose Renau, Proceedings of the **SPIE**, 2010.

[46] *Using Checkpoint-Assisted Value Prediction to Hide L2 Misses*, Luis Ceze, Karin Strauss, James Tuck, Jose Renau, and Josep Torrellas, ACM's Transactions on Architecture and Code Optimization (**TACO**), March 2006.

[47] *Energy-Efficient Thread-Level Speculation on a CMP*, Jose Renau, Karin Strauss, Luis Ceze, Wei Liu, Smruti Sarangi, James Tuck, and Josep Torrellas. IEEE Micro Special Issue: **Micro's Top Picks** from Computer Architecture Conferences, January-February 2006.

[48] *CAVA: Hiding L2 Misses with Checkpoint-Assisted Value Prediction*, Luis Ceze, Karin Strauss, James Tuck, Jose Renau, and Josep Torrellas, IEEE TCCA Computer Architecture Letters (**TCCA**), December 2004.

[49] *Managing Multiple Low-Power Adaptation Techniques: The Positional Approach*, Michael Huang, Jose Renau, Josep Torrellas, Sidebar, IEEE **Computer Magazine**, December 2003.
[50] *A Framework for Dynamic Energy Efficiency and Temperature Management*, Wei Huang, Jose Renau, and Josep Torrellas, Journal on Instruction Level Parallelism (**JILP**), October 2001.
[51] Oracle Patent, Combining a Remote TLB Lookup and a subsequent Cache Miss into a Single Coherence Operation. ORA12-0263-US-NP
[52] UCSC Patent application, Long Latency Tolerant Decoupled Memory Hierarchy for Simpler and Energy Efficient PCT/US2012/070046

Workshops and Posters

[53] LGraph: A Unified Data Model and API for Productive Open-Source Hardware Design, Sheng-Hong Wang, Rafael T. Possignolo, Qian Chen, Rohan Ganpati, and Jose Renau, Second Workshop on Open-Source EDA Technology (WOSET), November 2019.
[54] LNAST: A Language Neutral Intermediate Representation for Hardware Description Languages, Sheng-Hong Wang, Akash Sridhar, and Jose Renau, Second Workshop on Open-Source EDA Technology (WOSET), 2019.
[55] LGraph: A multi-language open-source database for VLSI, Rafael T. Possignolo, Sheng Hong Wang, Haven Skinner, and Jose Renau. First Workshop on Open-Source EDA Technology (WOSET), November 2018.
[56] Automating the Area-Delay Trade-off Problem, Haven Skinner, Rafael T. Possignolo, and Jose Renau. Second Workshop on Computer Architecture Research with RISC-V (CARRV), June 2018.
[57] *Anubis: A new benchmark for incremental synthesis*, Rafael Trapani Possignolo, Nursultan Kabylkas, and Jose Renau, International Workshop Logic and Synthesis (**IWLS**), June 2017.
[58] *LiveSynth: Towards an Interactive Synthesis Flow*, Rafael Trapani Possignolo, Jose Renau, Hot Chips A Symposium on High Performance Chips (HotChips poster), August 2016.
[59] *Fluid Pipelines: Elasticity without Throughput Penalty*, Rafael Trapani Possignolo, Elnaz Ebrahimi, Haven Skinner, and Jose Renau, International Workshop on Logic and Synthesis (**IWLS**), April 2016.
[60] *Section Based Program Analysis to Reduce Overhead of Detecting Unsynchronized Thread Communication*, Madan Das, Gabriel Southern, and Jose Renau, 20th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP Poster), February 2015
[61] *Deterministic Scaling*, Gabriel Southern, Madan Das, and Jose Renau, Workshop on Determinism and Correctness in Parallel Programming (WODET), March 2013.
[62] *Reducing Logging Overhead for Deterministic Execution*, Gabriel Southern, Madan Das, and Jose Renau, Workshop on Determinism and Correctness in Parallel Programming (WODET), March 2013.

[63] *ReRack: Power Simulation for Data Centers with Renewable Energy Generation*, Michael Brown, and Jose Renau, GreenMetrics 2011,held in conjunction SIGMETRICS 2011, June 2011.

[64] *SOI, Interconnect, Package, and Mainboard Thermal Characterization*, Joseph Nayfach-Battilana and Jose Renau, Poster with proceedings at International Symposium on Low Power Electronics and Design (ISLPED), August 2009.

[65] *Measuring and Modeling Variability using Low-Cost FPGAs*, Michael Brown, Cyrus Bazeghi, Matthew Guthaus and Jose Renau, Poster with Proceedings at the International Symposium on Field-Programmable Gate Arrays (FPGA), February 2009.

[66] *Measuring and Modeling Variability using Low-Cost FPGAs*, Michael Brown, Cyrus Bazeghi, Matthew R. Gutthaus, and Jose Renau, Workshop on Modeling, Benchmarking and Simulation (MOBS), held inconjunction with ISCA-36, June 2009.

[67] *Implementation of a Power Efficient High Performance FPU for SCOORE*, Wael Ali Ashmawi, John Burr, Abhishek Sharma, Jose Renau, Workshop on Architectural Research Prototyping (WARP) held in conjunction with ISCA, June 2008.

[68] *Measuring Power and Temperature from Real Processors*, Francisco-Javier Mesa-Martinez, Michael Brown, Joseph Nayfach-Battilana, Jose Renau, The Next Generation Software (NGS) Workshop (NGS08) held in conjunction with IPDPS, April 2008.

[69] *uDSim, a Microprocessor Design Time Simulation Infrastructure*, Sangeetha Sudhakrishnan, Francisco-Javier Mesa-Martinez, Jose Renau, Wild and Crazy Ideas VI (WACI) held in conjunction with ASPLOS, March 2008.

[70] *Printed Circuit Board Layout Time Estimation*, Cyrus Bazeghi and Jose Renau, 7th Workshop on Complexity-Effective Design (WCED), held in conjunction with ISCA-33, June 2006.

[71] *SCOORE: Santa Cruz Out-of-Order RISC Engine, FPGA Design Issues*, Francisco J. Mesa-Martinez, Abhishek Sharma, Andrew W. Hill, Carlos A. Cabrera, Cyrus Bazeghi, Hari Kolakaleti, Joseph Nayfach, Keertika Singh, Kevin S. Halle, Matthew D. Fischler, Melisa Nunez, Sangeetha Nair, Suraj Narender Kurapati, Wael Ali Ashmawi, and Jose Renau , Workshop on Architectural Research Prototyping (WARP), held in conjunction with ISCA-33, June 2006.

[72] *Profile-Based Energy Reduction for High Performance*, Wei Huang, Jose Renau, and Josep Torrellas, ACM Workshop on Feedback-Directed and Dynamic Optimization (FDDO), December 2001.

[73] *Energy/Performance Design of Memory Hierarchies for Processor-In-Memory Chips*, Wei Huang, Jose Renau, Seung-Moon Yoo, and Josep Torrellas, Workshop on Intelligent Memory Systems, November 2000. It also appeared in Lecture Notes in Computer Science (Vol. 2107) by Springer-Verlag, 2001.

[74] *Memory Hierarchies in Intelligent Memories: Energy/Performance Design*, Wei Huang, Jose Renau, Seung-Moon Yoo, and Josep Torrellas, Ninth Workshop on Scalable Shared Memory Multiprocessors, June 2000.

Profesional Activities and Memberships

- Maintain ESESC (https://github.com/masc-ucsc/esesc) used by academia and industry.
- Co-develop dromajo (https://github.com/chipsalliance/dromajo) used by academia and industry.
- General co-chair: HotChips 2017, WOSET 2020, 2021.
- Program Chair: ISPASS 2015, HotChips 2010 co-chair.
- Local/tutorial Chair: PPoPP/CGO/HPCA 2015, VLSI-SoC 2013, ISCA 2020.
- Associate editor from the IEEE Computer Architecture Letters since 2015.
- Program Committee service: ISCA 11,16,18; ISPASS 12,14,16; HPCA 14,23; SC 13; HotPower 10; MICRO 09,22; ICPP 09; HotChips 08,09,10; ICCD 06,07,08,09, IPDPS 07
- UCSC Host MURN Kickoff 2011, RAMP 2010
- Guest editor for IEEE MICRO March/April 2011 edition.
- NSF Panels: 2015, 2014, 2013, 2012, 2006
- RISC-V foundation memory consistency group.
- IEEE TCMM chair 2020-2023

Current and Past Employers – Professor Jose Renau

2004-current: **UC Santa Cruz** – Associate Professor

2013-2019: **Huawei** - Pathfinding, performance, prefetching, and verification for server-class out-of-order cores.

2015-current: **Imagination** - Design branch predictor, performance modeling

2017-current: **Esperanto Tech.** - Help in many aspects around out-of-order core and AI inference engine.

2020-2022: **Futurewei** - Performance modeling

2020-2021: **Alibaba** - Out-of-order core verification